mobilint

MLX-A1 Datasheet

Hardware Datasheet

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Document Revision History

Doc Revision Number	Date	Description
Ver. 1	Jul. 22, 2025	Initial Draft
Ver. 2	Sep. 30, 2025	Specification change
Ver. 3	Nov. 7, 2025	Specification change
Ver. 4	Mar. 23, 2026	Specification change

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1. Introduction

MLX-A1, Mobilint's embedded edge AI PC, is built for seamless integration into a wide range of system designs and edge AI application environments. At its core is the **ARIES-powered MLA100 Mobile Express Module (MXM)**, featuring four 64-bit U74 RISC-V cores and essential system components for scalable, reliable AI performance. Its compact form factor, low power consumption, and versatile I/O make the MLX-A1 a robust and efficient platform for intelligent edge computing.

ARIES is Mobilint's low-power, high-performance **Neural Processing Unit (NPU)** designed to deliver efficient AI acceleration in edge computing environments. Optimized for real-time inference, ARIES enables high-performance AI workloads even in resource-constrained systems such as smart cities, smart factories, autonomous robots, and AI surveillance devices.

Key features include:

- **Core-Local Interruptor (CLINT)** for local interrupt handling
- **Platform-Level Interrupt Controller (PLIC)** for system interrupt management and memory protection
- **Nexus 5001-compliant instruction trace** for non-intrusive debugging and performance profiling
- **Local crossbar interconnect** for efficient integration of functional units

The ARIES memory subsystem includes a directory-based coherence manager. All cache and memory units support Single Error Correction, Double Error Detection (SECDED) ECC, ensuring robust operation for safety-critical applications.

2. Specification

MLX-A1 Edge AI PC		
Model		MLX-A1
Motherboard		Aetina AIB-AHE5-A1
CPU		Intel i5-13600HE
NPU	NPU	MLA100 MXM (ARIES)
	Performance	80 TOPS
	Operating Freq.	1.25 GHz
	No. of Core	8
Graphics		Intel® Iris® Xe Graphics
Memory		DDR5 SO DIMM 16GB x2
Storage		2280 NVMe 512GB
LAN (Ethernet)		3 x 2.5Gbps
Interface	Rear I/O	· 4 x USB 2.0 · 2 x USB 3.2 · 1 x Power input connector · 1 x HDMI · 3 x RJ45 (LAN) · 1 x Reset button
	Front I/O	· 1 x Power Button (w/ LED)
BIOS Function		AMI EFI 256 Mbit, SPI
Software	OS	Ubuntu 22.04
Power Supply		DC 19.5V (Max 230W)
TDP		70W
Physical	Dimension	178 x 116 x 67mm
	Weight	1.3kg
Max Resolution	HDMI	4096 x 2304 @ 60Hz (HDMI 2.1)
Temperature	Operating	-20°C to 60°C with 0.5m/s air flow

Table 1 MLX-A1 Specification

3. Block Diagram

Refer to **Figure 1** for the block diagram of the MLA100 MXM card embedded within the MLX-A1 AI box.

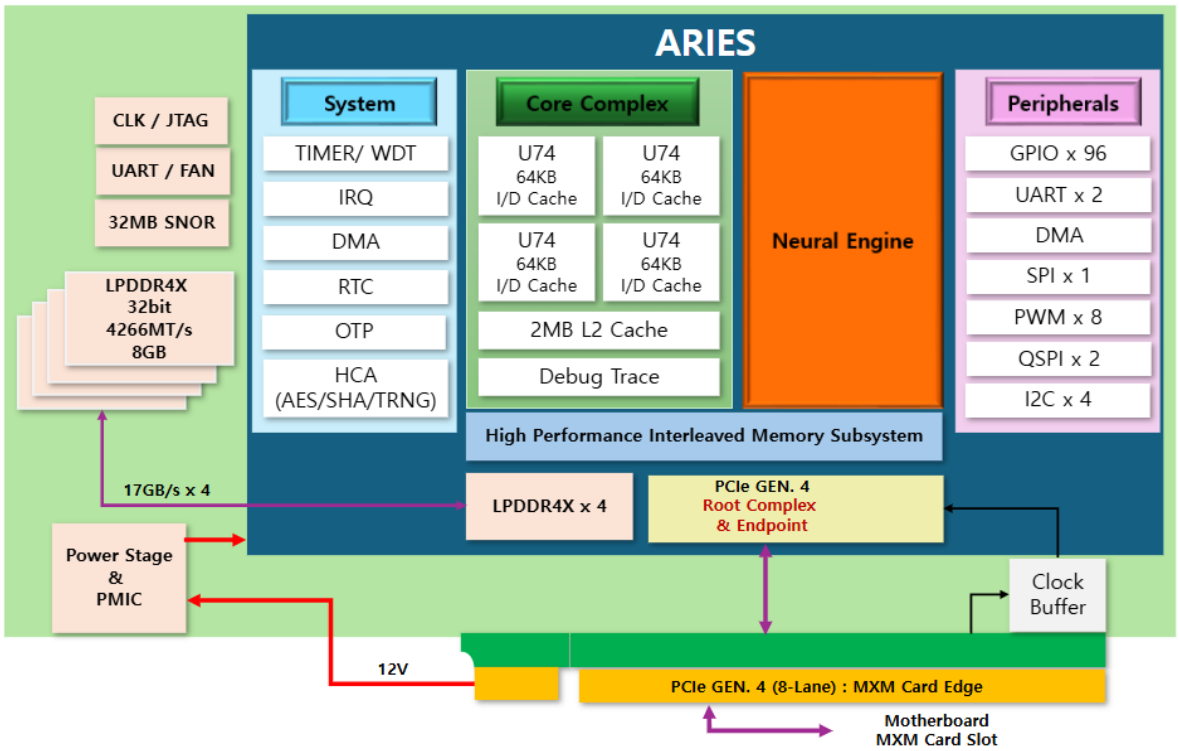

Figure 1 MLA100 MXM Block Diagram

Table 2 provides a summary of the key features of ARIES, the NPU AI accelerator that powers the AI capabilities of MLX-A1.

Feature	Description
Number of Harts	4 Harts
U74 Core	4 × U74 RISC-V cores
PLIC Interrupts	246 Interrupt signals, which can be connected to off-core complex devices
PLIC Priority Levels	The PLIC supports 7 priority levels.
Hardware Breakpoints	4 hardware breakpoints
Physical Memory Protection Unit	PMP with 8 regions and a minimum granularity of 4096 bytes

Table 2 ARIES Features Set

4. Features

1. **NPU PCIe**
   - PCIe Interface
     - Supports link rates of 2.5, 5.0, 8.0 and 16.0 GT/s per lane
     - 16-bit PIPE interface
     - Compliant with PHY Interface for PCIe (PIPE) Revision 4.4.1
     - PCIe® Base Specification Revision 4.0 v1.0 compliant
     - Designed for Endpoint silicon
     - Integrated Clock Domain Crossing (CDC) for flexible bridge clocking
     - Clock and power gating support
     - Native Active State Power Management L0s support
     - MSI and INT message support
     - MSI-X capability support
     - Address Translation Service, including Page Request interface
   - AXI Interface
     - An AXI4-Lite Slave interface for Bridge Configuration
     - An AXI4 Master interface, supporting up to 64 outstanding read and write requests
     - An AXI4 Slave interface, supporting up to 64 outstanding read requests and 8 outstanding write requests
     - 256-bit data support for AXI4 Master and Slave interfaces
   - Configuration
     - Bridge Configuration Space accessible by PCIe and/or AXI4-Lite Slave Interface
     - 4 KBytes for Bridge Internal Registers
     - 4 KBytes for PCIe Configuration Space
     - 8 KBytes dedicated to user-defined external registers in the AXI domain
     - Option to hardwire Bridge Internal Registers for a lower footprint
   - DMA Engines
     - Up to 4 fully independent DMA Engines
     - Up to 4 GBytes length transfers
     - Up to 64 outstanding read requests
     - Reconfigurable Source and Destinations, enabling targeting of PCIe, AXI4 Master input and output interfaces
   - Address Translation
     - Up to 16 reconfigurable address translation tables for PCIe interface
     - Up to 8 reconfigurable address translation tables per AXI4 Slave interface
     - Translated accesses can target PCIe, AXI4 Master interfaces

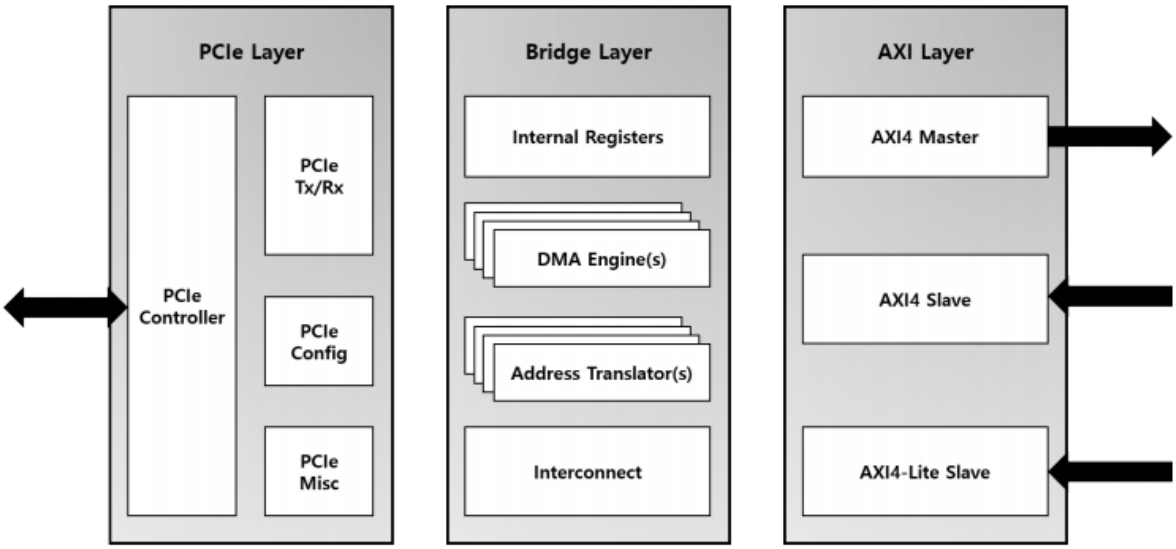

Figure 2 PCIe controller Block Diagram

2. LPDDR4/LPDDR4x Memory Subsystem

■ The subsystem instantiates memory controller and PHY IP to support maximum 2 ranks of 32-bit wide LPDDR4 up to 4267 MT/s.

- Compliant with LPDDR4 SDRAM Revision B up to 4267Mbps
  - Per-channel (x16) DRAM capacities supported: 2Gb, 3Gb, 4Gb, 6Gb, 8Gb, 12Gb, 16Gb
  - Supported burst length: 16 and 32, selectable on-the-fly
- Maximum two DRAM ranks
- Read/Write split request queue
- Bank interleaving
- Rank interleaving (symmetric ranks only)

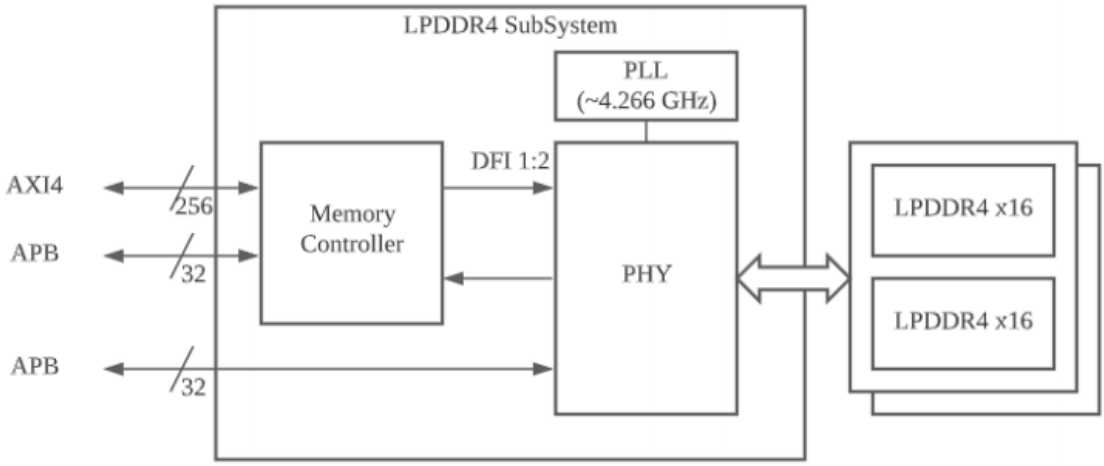

Figure 3 LPDDR4/LPDDR4x subsystem Block Diagram

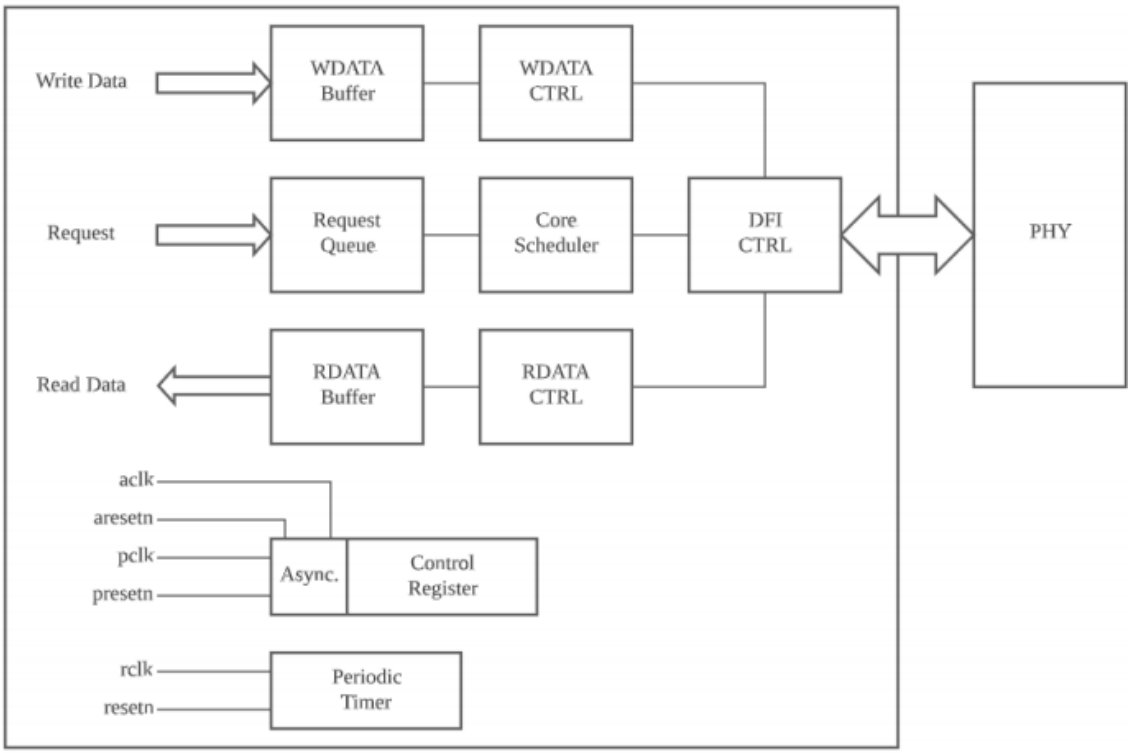

Figure 4 LPDDR4/LPDDR4x controller block diagram

3. **U74-MC Application Processor Complex**
   - Fully compliant with the RISC-V ISA specification
   - Quad RV64GC U74 Application Core
     - 32KB L1 I-cache with ECC
     - 32KB L1 D-cache with ECC
     - 8-region Physical Memory Protection
     - 256 Global Interrupts per core
     - Sv48 Virtual Memory support with 47-bit Physical Address
   - Integrated 2MB L2 cache with ECC
   - CLINT for timer/software interrupts
   - PLIC supports up to 246 interrupts with 7 priority levels
   - Benchmark Scores
     - 4.27/2.5 DMIPS/MHz (Best Effort / Legal)
     - 5.1 CoreMark/MHz

4. **Programmable Direct Memory Access (PDMA)**
   - The PDMA unit has memory-mapped control registers accessed over a TileLink slave interface to allow software to set up DMA transfers. It also has a TileLink bus master port connected to the TileLink bus fabric for automatic data-transfer between slave devices and main memory or for rapid data-copy between two locations in memory. The PDMA unit can support multiple independent DMA transfers simultaneously using different PDMA channels and can generate PLIC interrupts on various conditions during DMA execution.
   - ARIES PDMA has 4 independent DMA channels, which operate concurrently to support multiple simultaneous transfers
   - The PDMA has 2 interrupts per channel to signal either transfer completion or

transfer error

5. **Process, Voltage, Temperature Sensor (PVT)**
   - Integrated on-chip PVT sensor
   - 12-bit digital output resolution
   - Junction temperature monitoring with 0.0625°C/code precision
   - Operating temperature range: –40°C to +125°C
   - Includes internal thermal probe and analog-to-digital converter
   - Supports remote temperature sensing via external probes

6. **I2C Interface**
   - The Two-wire serial interface: SDA (data) and SCL (clock)
   - Supports multiple device roles: master/slave, transmitter/receiver
   - Each device has a unique address for bus arbitration
   - Supported modes:
     - Standard Mode: up to 100 Kb/s
     - Fast Mode: up to 400 Kb/s
     - Fast Mode Plus: up to 1 Mb/s
     - High Speed Mode: up to 3.4 Mb/s
     - Ultra-Fast Mode (write-only, no ACK): up to 5 Mb/s

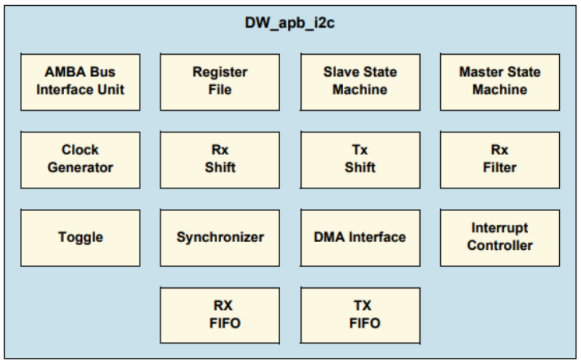

Figure 5 I2C Block Diagram

7. **Universal Asynchronous Receiver/Transmitter (UART)**
   - 8-N-1 and 8-N-2 formats: 8 data bits, no parity bit, 1 start bit, 1 or 2 stop bits.
   - 8-entry transmit and receive FIFO buffers with programmable watermark interrupts.
   - 16× Rx oversampling with 2/3 majority voting per bit.
   - Limitations: Does not support hardware flow control, other modem control signals, or synchronous serial data transfers

8. **Pulse Width Modulation (PWM)**
9. **SPI, QSPI**
10. **General Purpose I/O (GPIO)**
11. **Watchdog Timer (WDT)**
12. **One-Time Programmable Memory (OTP)**
13. **PRCI (Power Reset Clocking Interrupt)**
14. **Power Domain**

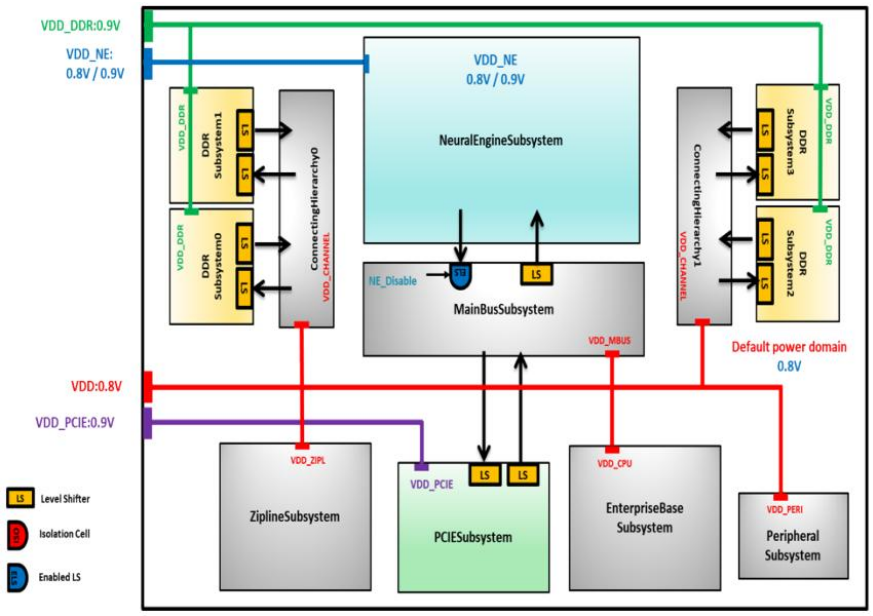

Figure 6 ARIES (Power Domain)

5. Product Layout

5.1. Product Dimensions

Figure 7 shows the dimensions of MLX-A1 embedded AI PC.

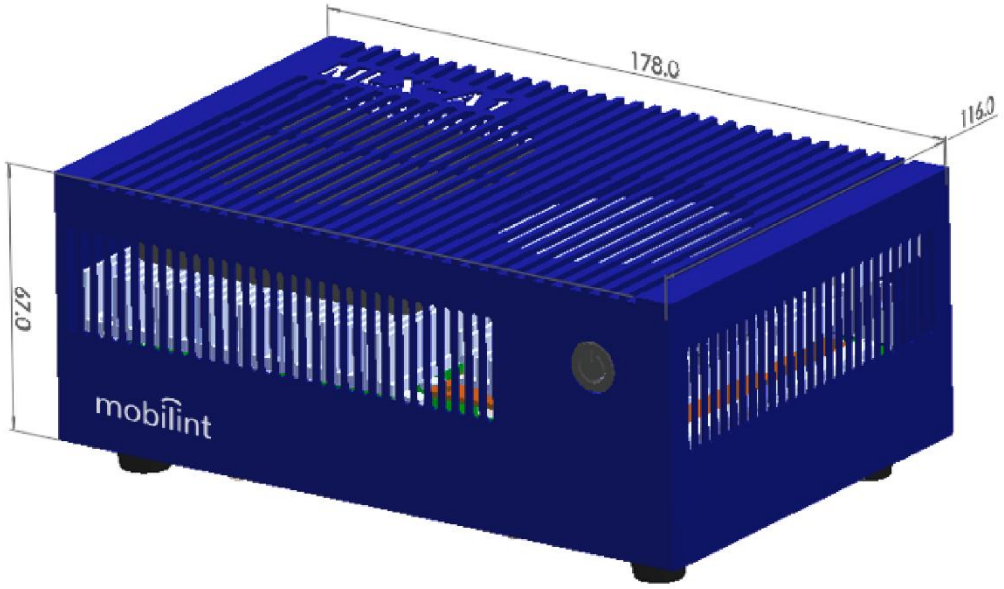

Figure 7 MLX-A1 Dimensions

5.2. I/O Interfaces

The following figures show the input and output interfaces supported by the MLX-A1 embedded AI PC.

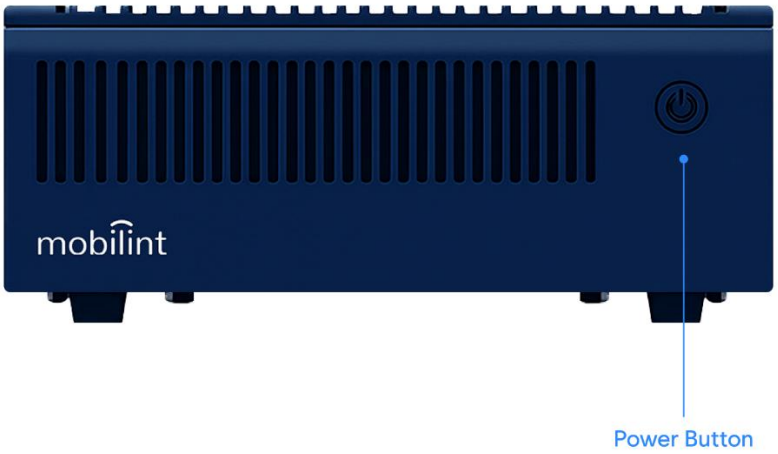

Figure 8 MLX-A1 I/O Interfaces – Front View

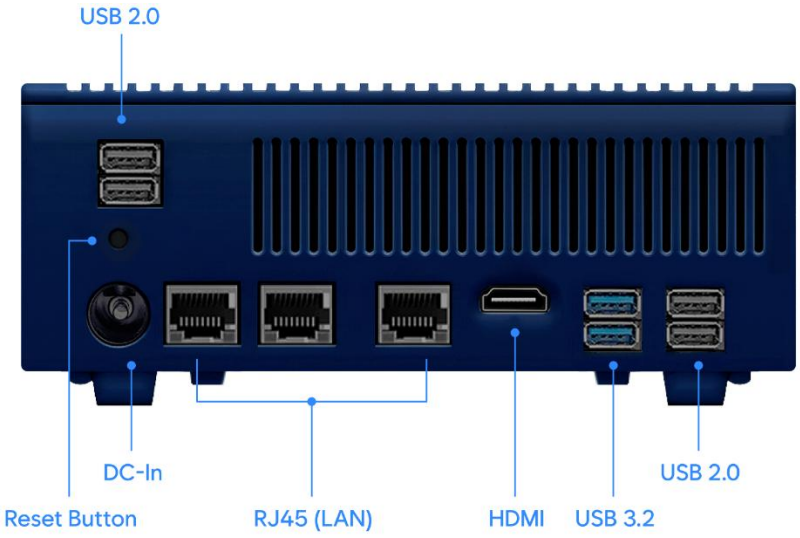

Figure 9 MLX-A1 I/O Interfaces – Rear View

6. Installation

6.1. Instructions

1. Ensure all necessary components (power adapter, peripherals, cables, etc.) are present.
2. Connect the peripherals, including display, cameras or sensors, keyboard and mouse, and ethernet.

3. Connect the power adapter to the AI PC.
4. Power on the system.
5. The system will boot into Ubuntu 22.04 OS, preinstalled with the driver and runtime components of SDK qb, Mobilint's proprietary software development kit.
6. For further software references, refer to Section 6.4. Software Installation.

6.2. Important Notes Before Installation

1. The installation instructions above are for reference only. Actual installation may vary depending on the system environment.
2. Before operating the product, discharge any static electricity from your body by touching a metal frame.
3. Handle the product by its chassis and avoid contact with circuitry or connector.
4. Ensure that clothing or accessories do not come in contact with electronic components.

6.3. Warnings and Cautions

1. Do not connect or disconnect the product while the system is powered on.
2. Do not disassemble or modify the product without proper guidance. This may result in product damage, electric shock, or other unexpected hazards.
3. Do not touch the product with wet hand(s) to prevent electric shock.
4. Operating the product in environments with high humidity or insufficient ventilation may reduce its lifespan.
5. Ensure that water or other liquids do not come in contact with the product, as this may cause serious damage.
6. Keep the product in its storage packaging box when not in use.

6.4. Software Installation

For a comprehensive guide to fully utilizing the software stack for MLX-A1, refer to the following resources available in Mobilint's documentation page (docs.mobilint.com) and the Distribution Site (dl.mobilint.com), where you can also find the files and modules necessary to run Mobilint's NPU products.

File Type	Document Title	Available Languages
Compiler	qb Compiler Manual	English
Runtime Library	qb Runtime Manual	English
Driver	Windows Driver Manual	English, Korean
Driver	Linux Driver Manual	English, Korean

Table 3 Mobilint SDK qb Resources

For inquiries and further technical support, please contact us through our official support channel.

- Support Channel: tech-support@mobilint.com

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