mobilint

MLA100 MXM Datasheet

Hardware Datasheet

MAH005-02-001 Version 2
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Document Revision History

Doc Revision Number	Date	Description
Version 1	Oct. 27, 2025	Initial Draft
Version 1.1	Jan. 28, 2026	Added Operation Temperature
Version 2	Feb. 6, 2026	- Product name unification - Software instruction updated

Table of Contents

1. Introduction

ARIES is Mobilint's low-power, high-performance **Neural Processing Unit (NPU)** designed to deliver efficient AI acceleration in edge computing environments. Optimized for real-time inference, ARIES enables high-performance AI workloads even in resource-constrained systems such as smart cities, smart factories, autonomous robots, and AI surveillance devices.

MLA100 MXM, powered by ARIES, is a mobile express module allowing seamless integration into a variety of system designs and application environments. Integrating **four 64-bit U74 RISC-V cores** along with essential system components, the ARIES-powered MLA100 MXM supports reliable and scalable AI processing.

Key features include:

- **Core-Local Interruptor (CLINT)** for local interrupt handling
- **Platform-Level Interrupt Controller (PLIC)** for system interrupt management and memory protection
- **Nexus 5001-compliant instruction trace** for non-intrusive debugging and performance profiling
- **Local crossbar interconnect** for efficient integration of functional units

The ARIES memory subsystem includes L1 instruction and data caches, a shared L2 cache, and a directory-based coherence manager. All cache and memory units support Single Error Correction, Double Error Detection (SECDED) ECC, ensuring robust operation for safety-critical applications.

2. Block Diagram

Refer to **Figure 1** for the block diagram of the MLA100 MXM form factor.

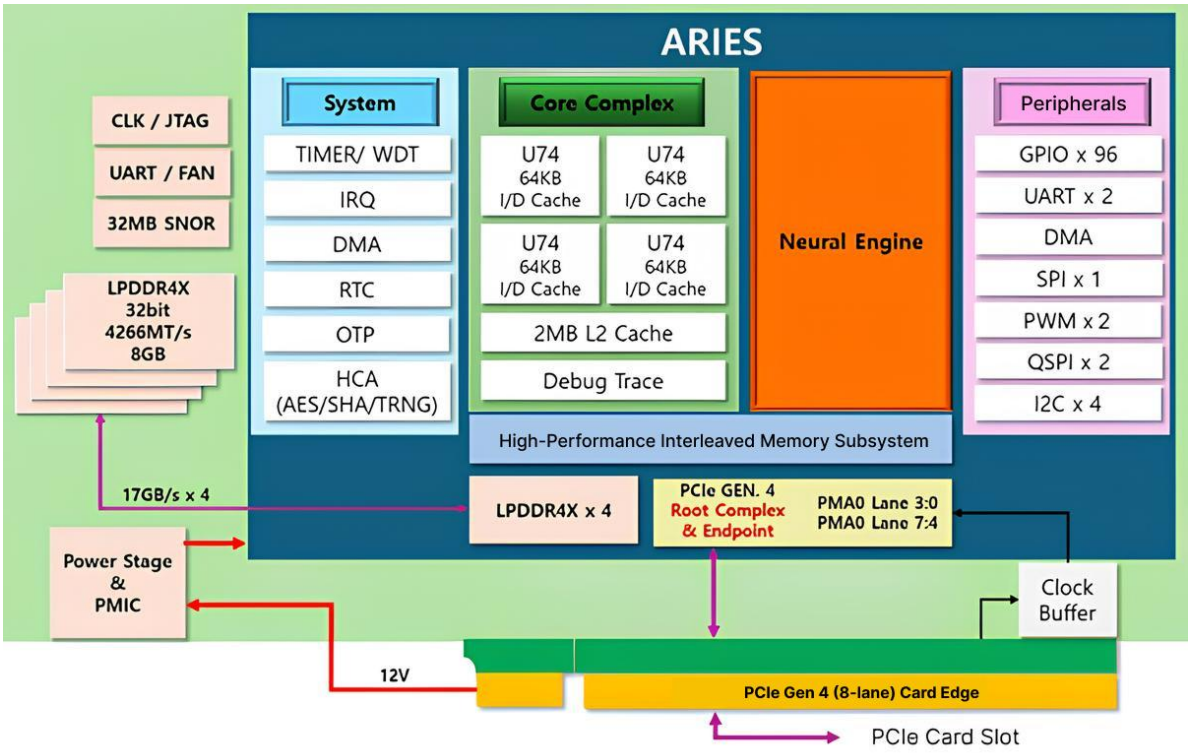

Figure 1 ARIES-Powered MLA100 MXM Block Diagram

Table 1 provides a summary of the key features of ARIES.

Table 1 ARIES Features Set

Feature	Description
Number of Harts	4 Harts
U74 Core	4 × U74 RISC-V cores
PLIC Interrupts	246 Interrupt signals, which can be connected to off-core complex devices
PLIC Priority Levels	The PLIC supports 7 priority levels.
Level 2 Cache	2 MB 16-way L2 Cache
Hardware Breakpoints	4 hardware breakpoints
Physical Memory Protection Unit	PMP with 8 regions and a minimum granularity of 4096 bytes

3. Features

1. **PCIe**
   - ■ PCIe Interface
     - ➢ Supports link rates of 2.5, 5.0, 8.0 and 16.0 GT/s per lane
     - ➢ 16-bit PIPE interface
     - ➢ Compliant with PHY Interface for PCIe (PIPE) Revision 4.4.1
     - ➢ PCIe® Base Specification Revision 4.0 v1.0 compliant
     - ➢ Designed for Endpoint silicon
     - ➢ Integrated Clock Domain Crossing (CDC) for flexible bridge clocking
     - ➢ Clock and power gating support
     - ➢ Native Active State Power Management L0s support
     - ➢ MSI and INT message support
     - ➢ MSI-X capability support
     - ➢ Address Translation Service, including Page Request interface
   - ■ AXI Interface
     - ➢ An AXI4-Lite Slave interface for Bridge Configuration
     - ➢ An AXI4 Master interface, supporting up to 64 outstanding read and write requests
     - ➢ An AXI4 Slave interface, supporting up to 64 outstanding read requests and 8 outstanding write requests
     - ➢ 256-bit data support for AXI4 Master and Slave interfaces
   - ■ Configuration
     - ➢ Bridge Configuration Space accessible by PCIe and/or AXI4-Lite Slave Interface
     - ➢ 4 KBytes for Bridge Internal Registers
     - ➢ 4 KBytes for PCIe Configuration Space
     - ➢ 8 KBytes dedicated to user-defined external registers in the AXI domain
     - ➢ Option to hardwire Bridge Internal Registers for a lower footprint
   - ■ DMA Engines
     - ➢ Up to 4 fully independent DMA Engines
     - ➢ Up to 4 GBytes length transfers
     - ➢ Up to 64 outstanding read requests
     - ➢ Reconfigurable Source and Destinations, enabling targeting of PCIe, AXI4 Master input and output interfaces
   - ■ Address Translation
     - ➢ Up to 16 reconfigurable address translation tables for PCIe interface
     - ➢ Up to 8 reconfigurable address translation tables per AXI4 Slave interface
     - ➢ Translated accesses can target PCIe, AXI4 Master interfaces

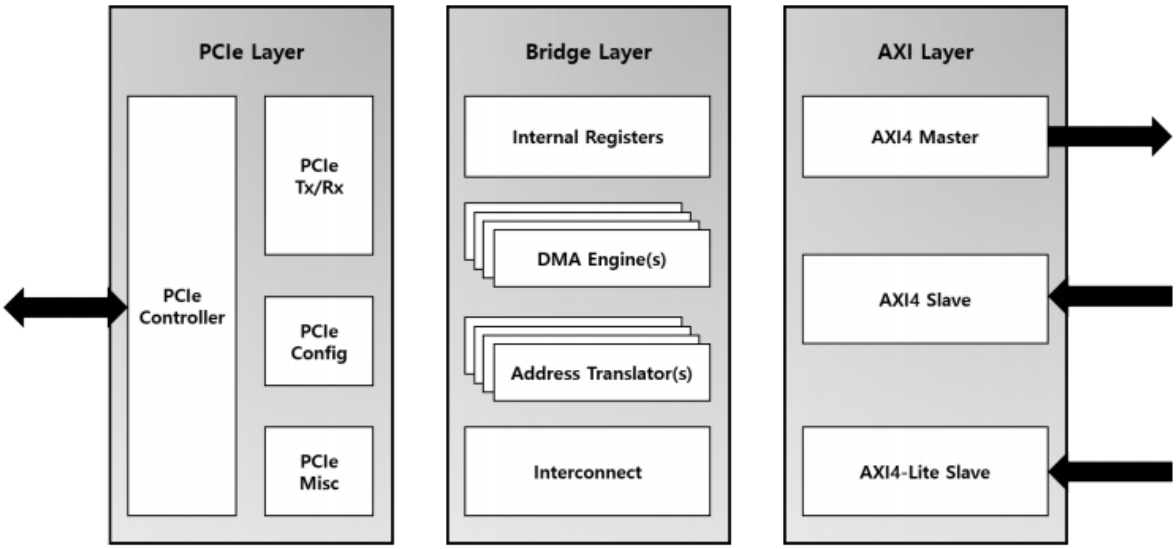

Figure 2 PCIe controller Block Diagram

2. LPDDR4/LPDDR4x Memory Subsystem

■ The subsystem instantiates memory controller and PHY IP to support maximum 2 ranks of 32-bit wide LPDDR4 up to 4267 MT/s.

- Compliant with LPDDR4 SDRAM Revision B up to 4267Mbps
  - Per-channel (x16) DRAM capacities supported: 2Gb, 3Gb, 4Gb, 6Gb, 8Gb, 12Gb, 16Gb
  - Supported burst length: 16 and 32, selectable on-the-fly
- Maximum two DRAM ranks
- Read/Write split request queue
- Bank interleaving
- Rank interleaving (symmetric ranks only)

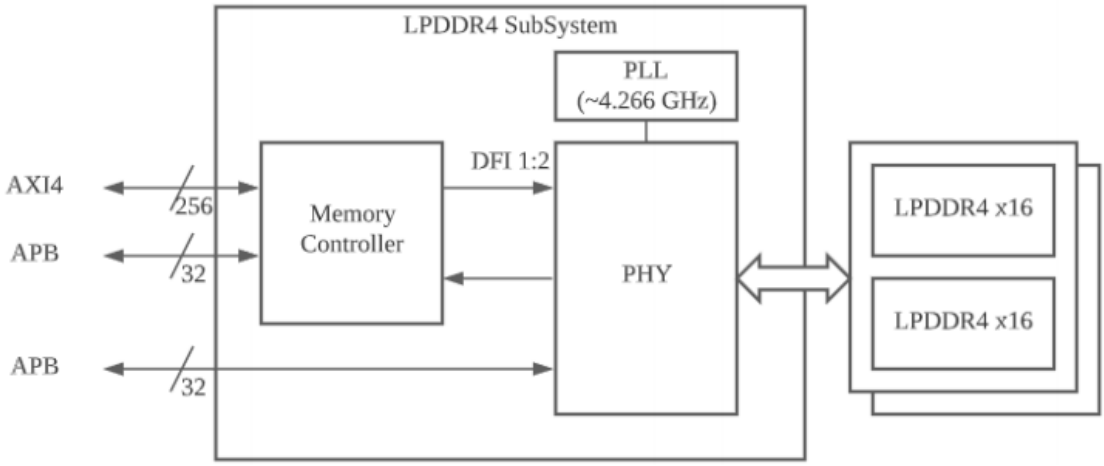

Figure 3 LPDDR4/LPDDR4x subsystem Block Diagram

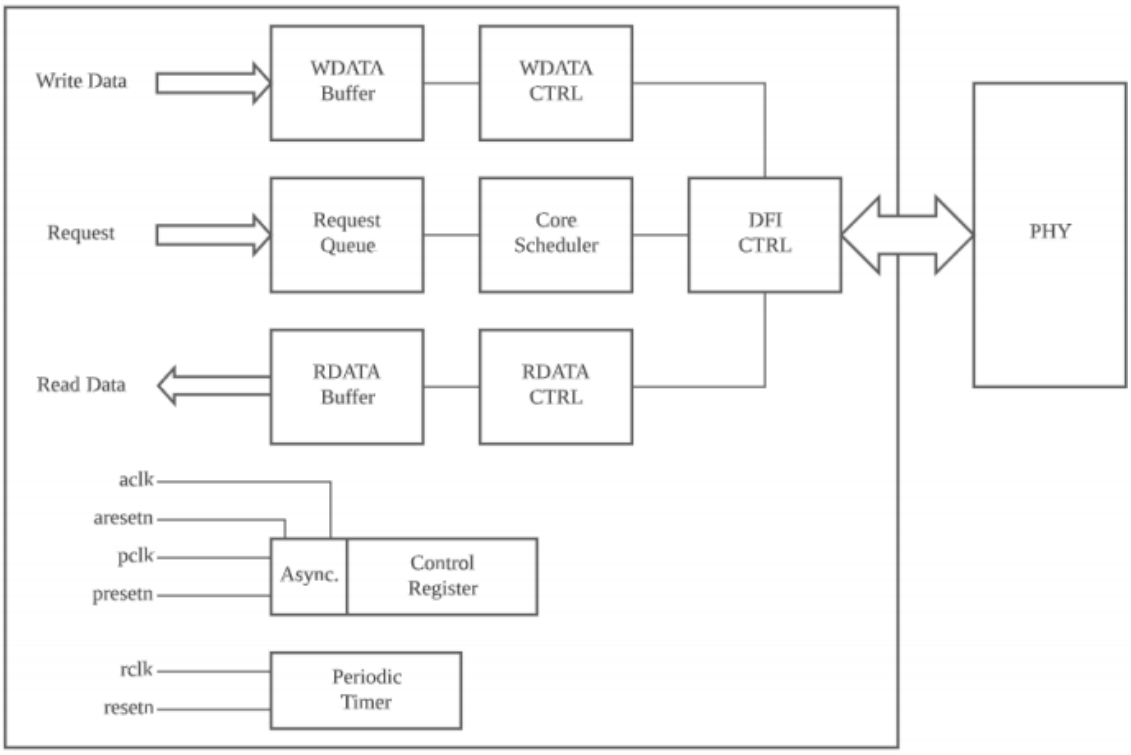

Figure 4 LPDDR4/LPDDR4x controller block diagram

3. **U74-MC Application Processor Complex**
   - Fully compliant with the RISC-V ISA specification
   - Quad RV64GC U74 Application Core
     - 32KB L1 I-cache with ECC
     - 32KB L1 D-cache with ECC
     - 8-region Physical Memory Protection
     - 256 Global Interrupts per core
     - Sv48 Virtual Memory support with 47-bit Physical Address
   - Integrated 2MB L2 cache with ECC
   - CLINT for timer/software interrupts
   - PLIC supports up to 246 interrupts with 7 priority levels
   - Benchmark Scores
     - 4.27/2.5 DMIPS/MHz (Best Effort / Legal)
     - 5.1 CoreMark/MHz

4. **Programmable Direct Memory Access (PDMA)**
   - The PDMA unit has memory-mapped control registers accessed over a TileLink slave interface to allow software to set up DMA transfers. It also has a TileLink bus master port connected to the TileLink bus fabric for automatic data-transfer between slave devices and main memory or for rapid data-copy between two locations in memory. The PDMA unit can support multiple independent DMA transfers simultaneously using different PDMA channels and can generate PLIC interrupts on various conditions during DMA execution.
   - ARIES PDMA has 4 independent DMA channels, which operate concurrently to support multiple simultaneous transfers
   - The PDMA has 2 interrupts per channel to signal either transfer completion or

transfer error

5. **Process, Voltage, Temperature Sensor (PVT)**
   - Integrated on-chip PVT sensor
   - 12-bit digital output resolution
   - Junction temperature monitoring with 0.0625°C/code precision
   - Operating temperature range: –40°C to +125°C
   - Includes internal thermal probe and analog-to-digital converter
   - Supports remote temperature sensing via external probes

6. **I2C Interface**
   - The Two-wire serial interface: SDA (data) and SCL (clock)
   - Supports multiple device roles: master/slave, transmitter/receiver
   - Each device has a unique address for bus arbitration
   - Supported modes:
     - Standard Mode: up to 100 Kb/s
     - Fast Mode: up to 400 Kb/s
     - Fast Mode Plus: up to 1 Mb/s
     - High Speed Mode: up to 3.4 Mb/s
     - Ultra-Fast Mode (write-only, no ACK): up to 5 Mb/s

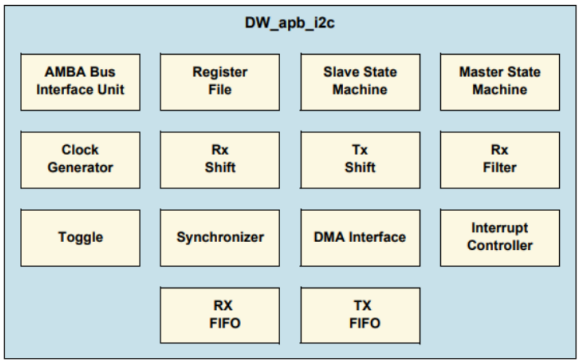

Figure 5 I2C Block Diagram

7. **Universal Asynchronous Receiver/Transmitter (UART)**
   - 8-N-1 and 8-N-2 formats: 8 data bits, no parity bit, 1 start bit, 1 or 2 stop bits.
   - 8-entry transmit and receive FIFO buffers with programmable watermark interrupts.
   - 16× Rx oversampling with 2/3 majority voting per bit.
   - Limitations: Does not support hardware flow control, other modem control signals, or synchronous serial data transfers

8. **Pulse Width Modulation (PWM)**
9. **SPI, QSPI**
10. **General Purpose I/O (GPIO)**
11. **Watchdog Timer (WDT)**
12. **One-Time Programmable Memory (OTP)**
13. **PRCI (Power Reset Clocking Interrupt)**
14. **Power Domain**

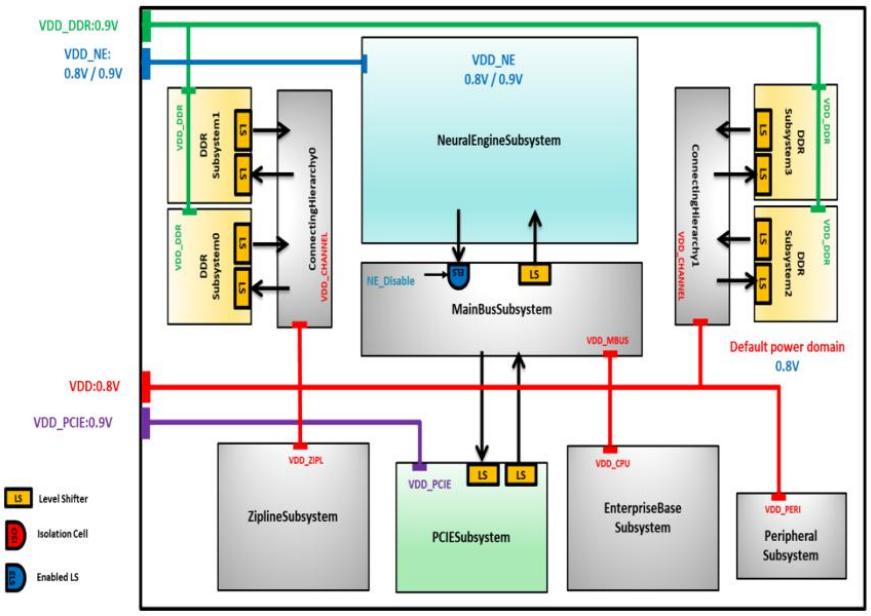

Figure 6 ARIES (Power Domain)

4. Specification

Table 2 MLA100 MXM Specification

Item		
Processor		RISC-V
NPU	NPU	ARIES
	Operating Freq.	1.25 GHz
	No. of Core	8
DDR	Model	LPDDR4X
	Operating Speed	4266 MT/s
	Capacity	4 Gbytes x 4
Flash Memory		128 Mbytes
PCIe		Gen4 8-lane
Console		1 port (UART to USB)
LED		2 (Power LED, Heartbeat LED)
Power		DC +12V (No External Power)
Size		(Type A) 82mm x 70mm
Power Consumption (TDP)		25W
Operating Temp.	**Standard Operation**	-35 to 65℃
	Extended Operation	-35 to 75℃
Storage Temp.		-55 to 85℃
Humidity		90℃ / 95%R.H Non-condensing

5. Dimension

The following figures show the dimensions of MLA100 MXM.

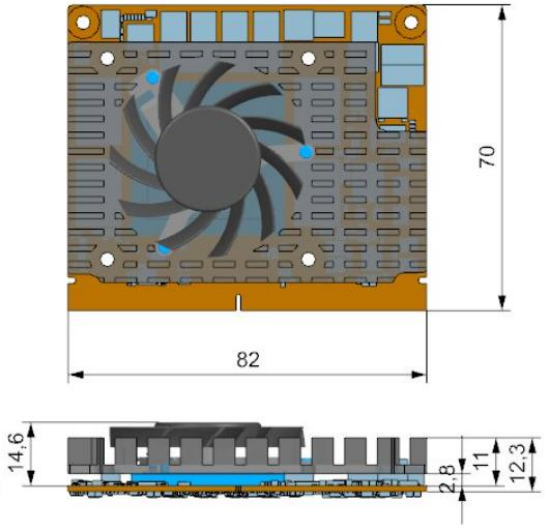

Figure 6 MLA100 MXM Dimensions (As-Is)

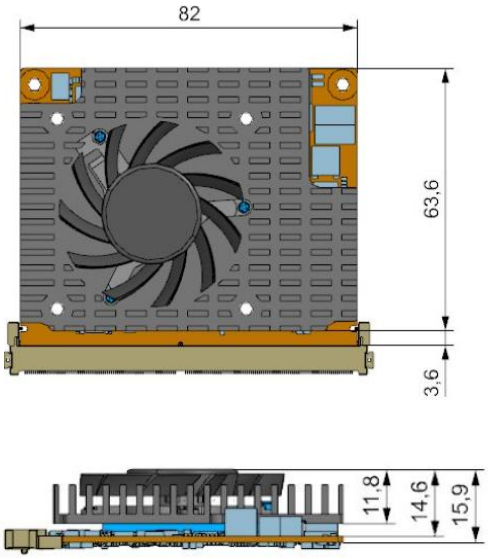

Figure 7 MLA100 MXM Dimensions (Installed in MXM Card Slot)

6. Appearance

Figure 8 MLA100 MXM Product Appearance - Front and Back

7. Installation

7.1. Instructions

1. Please ensure that the system power cable is disconnected before installing or removing the product.
2. Align the module pins with the motherboard's slot in the right direction.
3. Ensure that clothing or accessories do not come in contact with electronic components.
4. Insert the module at a 20° angle, then gently push it in to secure it in the slot.
5. Press down on the end of the module and fasten it firmly using the provided screws. Secure the other side with a screw as well.
6. Check that the module is firmly seated in the slot.
7. The MXM module comes with a pre-installed heatsink for effective thermal management. No additional installation is needed.

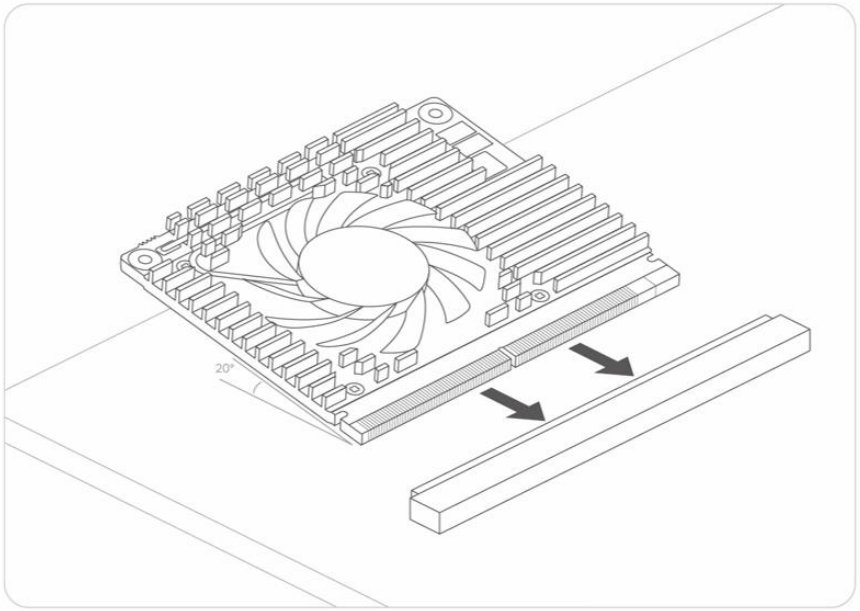

Figure 9 MLA100 MXM Installation

7.2. Important Notes Before Installation

1. The installation image above is for reference only. Actual installation may vary depending on the system environment.
2. Do not force the module into an incompatible slot.
3. Before installing the product, discharge any static electricity from your body by touching the metal frame inside the powered-off system.
4. Handle the product by its edges to avoid contact with circuitry or the PCIe connector.
5. Ensure that clothing or accessories do not come in contact with electronic components.

7.3. Warnings and Cautions

1. Do not connect or disconnect the product while the system is powered on.
2. Keep your hands, tools, or cables away from the fan while it is in operation. Ensure the fan has come to a complete stop before removing the product.
3. Do not disassemble or modify the product without proper guidance. This may result in product damage, electric shock, or other unexpected hazards.
4. Do not touch the product with wet hand(s) to prevent electric shock.
5. Operating the product in environments with high humidity or insufficient ventilation may reduce its lifespan.
6. Ensure that water or other liquids do not come in contact with the product, as this may cause serious damage.
7. Keep the product in its storage packaging box when not in use.

7.4. Software Installation

MLA100 MXM is operable with Mobilint's official software kit, SDK qb. The files and modules for SDK qb are available in our official support channels below:

· Download Center: https://dl.mobilint.com (requires user sign-up via support channel)

· Support Channel: tech-support@mobilint.com

For a comprehensive guide to software installation for MLA100 MXM, refer to the following resources available in Mobilint's documentation page (docs.mobilint.com).

File Type	Document Title	Available Languages
Compiler	qb Compiler Manual* *Only available in Download Center	English, Korean
Runtime Library	Runtime Library Manual	English, Korean
Driver	Windows Driver Manual	English, Korean
Driver	Linux Driver Manual	English, Korean

Table 3 Mobilint SDK qb Resources

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